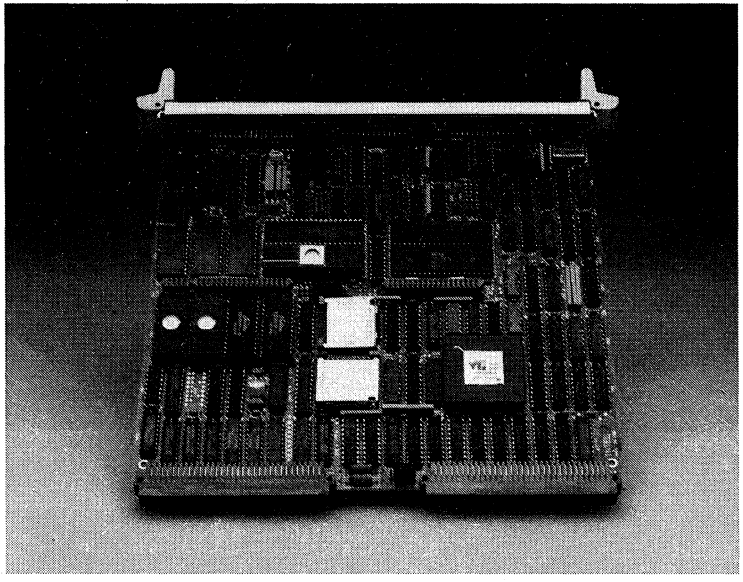
iSBC® 286/100A MULTIBUS®II SINGLE BOARD COMPUTER

- 8 MHz 80286 Microprocessor with Optional 80287 Numeric Data Co-Processor
- MULTIBUS® II iPSB (Parallel System Bus) Interface with Full Message Passing Capabilities and up to 4 Gigabytes of Memory Addressability on the Bus
- High-Speed Memory Expansion with MULTIBUS II iLBX II (Local Bus Extension) Interface Addresses up to 16 MBytes of Local and/or Dual Port Memory
- Two iSBX Bus Interface Connectors for I/O Expansion Bus
- Four DMA Channels Supplied by the 82258 Advanced DMA Controller with 8 MBytes/sec Transfer Rate
- MULTIBUS® II Interconnect Space for Software Configurability and Self-Test Diagnostics
- Resident Firmware Supports Self-Test Power-Up Diagnostics and On-Command Extended Self-Test Diagnostics
- Two Programmable Serial Interfaces, one RS232C (DCE or DTE), the other RS232C or RE422A/RS449 Compatible
- Two 28-pin JEDEC Sites for up to 128 KBytes of Local Memory Using SRAM, NVRAM, EEPROM, and EPROM
- 24 Programmable I/O Lines Configurable as SCSI Interface, Centronics Interface, or General Purpose I/O

The iSBC 286/100A Single Board Computer is part of Intel's family of MULTIBUS II CPU boards that utilizes the advanced features of the MULTIBUS II System Architecture. It is ideally suited for a wide range of OEM applications. The combination of the 80286 CPU, the Message Passing Coprocessor (MPC), the MULTIBUS II Parallel System Bus (iPSB bus), and the Local Bus Extension (iLBX II bus) makes the iSBC 286/100A board suited for high performance, multiprocessing system applications in a multimaster environment. The board is a complete microcomputer system on a 220mm x 233mm (8.7 x 9.2 inch) Eurocard form factor with pin and socket DIN connectors.



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Overview

The iSBC 286/100A Single Board Computer combines the 80286 microprocessor with the Message Passing Component (MPC) on a single board within the MULTIBUS II system architecture. This offers a message passing based high performance multiprocessing solution for system integrators and designers. Figure 1 shows a typical MULTIBUS II multiprocessing system configuration. Overall system performance is enhanced by the Local Bus Extension (iLBX II) which allows 0 wait state high speed memory execution.

Architecture

All features of the MULTIBUS II architecture are fully supported by the iSBC 286/100A board including the Parallel System Bus (iPSB), interconnect space, Built-In-Self-Tests (BIST) diagnostics, and full message passing. These features are described in the following sections. In addition to taking advantage of the MULTIBUS II system architecture, the iSBC 286/100A board has complete single board computer capability including two iSBX bus expansion connectors, 80287 numeric data coprocessor option, advanced DMA control, JEDEC memory sites, SCSI configurable parallel interface, serial I/O, and programmable timers. Figure 2 shows the iSBC 286/100A board block diagram.

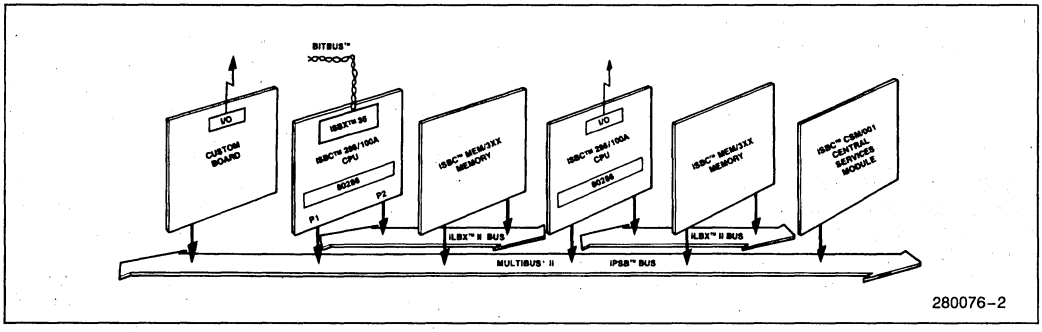

Figure 1. Typical MULTIBUS®II Multiprocessing System Configuration

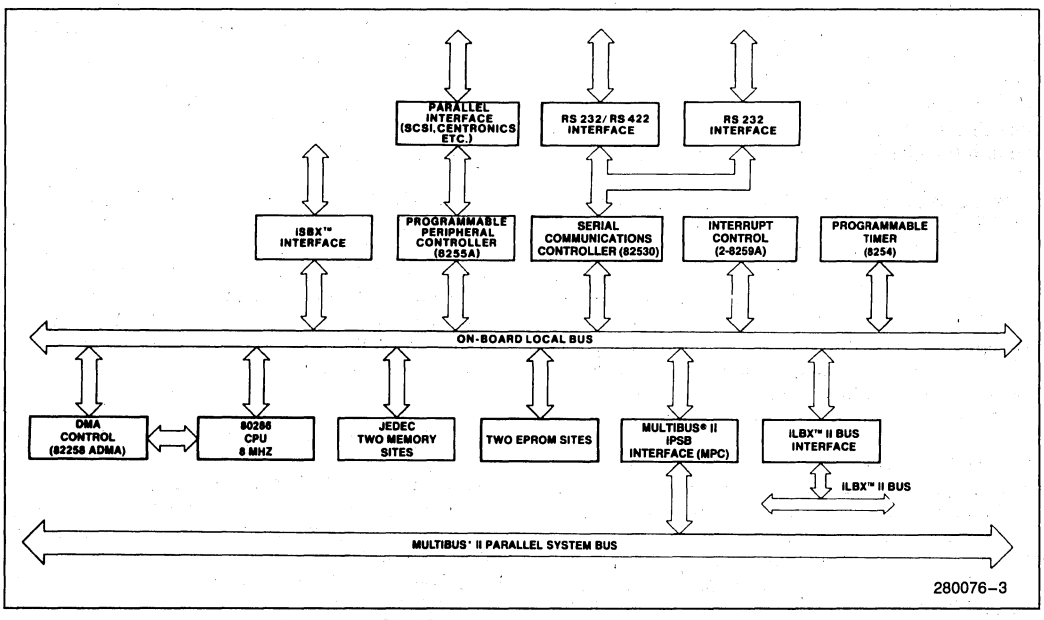

Figure 2. iSBC® 286/100A Board Block Diagram

Central Processing Unit

The central processing unit for the iSBC 286/100A board is the 80286 microprocessor operating at 8.0 MHz clock rate. The 80286 runs 8086 and 80186 code at substantially higher speeds (due to a parallel chip architecture) while maintaining software compatibility with Intel's 8086 and 80186 microprocessors. Numeric processing power may be enhanced with the 80287 numeric data coprocessor. The 80286 CPU operates in two modes: real address mode and protected virtual address mode. In real address mode, programs use real addressing with up to one megabyte of address space. In protected virtual address mode, the 80286 CPU automatically maps 1 gigabyte of virtual address per task into a 16 megabyte real address space. This mode also provides the hardware memory protection for the operating system. The operating mode is selected via CPU instructions.

iPSB Bus Interface

The iSBC 286/100A board has a Message Passing Coprocessor (MPC) component on the base board that contains most of the logic required to operate the Parallel System Bus (iPSB bus) interface. Some of the key functions provided by the MPC include bus arbitration, transfer control, parity generation and checking, and error detection and reporting.

Data transfers between processors via the iPSB bus is defined in the MULTIBUS II architecture through a transfer protocol, a reserved address space, and an information/data block. This interprocessor communication convention is known as message passing. Operations occurring within the reserved address space are called message space operations.

Message passing allows iPSB bus agents to transfer variable amounts of data at rates approaching the maximum bandwidth of the bus. Message passing permits a sustained transfer rate of 2.2 Mbytes per second, and a single message may transfer up to 16 Mbytes from one agent to another. The MPC fully supports message space operations, executes iPSB bus arbitration and executes the message passing protocol independent of the host CPU, leaving the host free to process other tasks.

The MPC supports both solicited and unsolicited message passing capability across the iPSB. An unsolicited message can be thought of as an intelligent interrupt from the perspective of the receiving agent because the arrival of an unsolicited message is unpredictable. Attached to an unsolicited message is one of 255 possible source addresses along with 28 bytes of data attached to the message data field. A solicited message moves large blocks of data between agents on the iPSB bus. The arrival of a solicited message is negotiated between the sending and receiving agents. Data is sent in "packets" with each packet containing four bytes of control information and up to 28 bytes of data. There is no specific limit to the number of packets that may be sent in a single message, but the total message may not transfer more than 16 Mbytes.

The iSBC 286/100A also includes a feature called the iPSB window register that allows the user to selectively access under software control any 256K byte block of memory within the 4 Gigabytes of memory space on the iPSB bus interface.

INTERCONNECT SPACE SUPPORT

Interconnect space is one of four MULTIBUS II address spaces, the other three being memory space, I/O space, and message space. Interconnect space allows software to initialize, identify, configure, and diagnose the boards in a MULTIBUS II system. The Interconnect template consists of 8-bit registers, organized into functional groups called records. There are three types of records, the header record, the function record, and the End of Template record.

The header record provides board and vendor ID information, general status and control information, and diagnostic control. The function record allows the user to configure and/or read the iSBC 286/100A board's hardware configuration via software. The End of Template record identifies the end of the interconnect template.

BUILT IN SELF TEST (BIST) DIAGNOSTICS

MULTIBUS II's Built in Self Test (BIST) diagnostics improve the reliability and error reporting and recovery capability of MULTIBUS II boards. These confidence tests and diagnostics not only improve reliability but also reduce manufacturing and maintenance costs for the OEM user. A yellow LED (LED 1) on the front panel provides a visual indication of the power-up diagnostics status.

Error Reporting and Recovery

The MULTIBUS II Parallel System Bus and the iLBX II bus provides bus transmission and bus parity error detection signals. Error information is logged in the MPC and a bus error interrupt is generated. Information on the error source for reporting or recovery purposes is available to software through the iSBC 286/100A board interconnect space registers.

INTERRUPT CONTROL

In a MULTIBUS II system, external interrupts (interrupts originating off the CPU board) are messages over the bus rather than signals on individual lines. Message based interrupts are handled by the MPC. Two on-board 8259A Programmable Interrupt Controllers (PICs) are used for processing on-board interrupts. One is used as the master and the other as the slave. Table 1 includes a list of devices and functions supported by interrupts.

iSBX® BUS MULTIMODULE™ ON-BOARD EXPANSION

Two iSBX bus MULTIMODULE connectors are provided, one 16- or 8-bit and the other 8-bit. Through these connectors additional on-board I/O functions may be added. The iSBX bus MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, and graphics control. The iSBX bus connectors on the iSBC 286/100A board provides all signals necessary to interface to the local on-board bus including 16 data lines and DMA for maximum data transfer rates. MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX bus connectors are also supported. A broad range of iSBX bus MULTIMODULE options are available from Intel. Custom iSBX bus MULTIMODULE boards designed for MULTIBUS or proprietary bus systems are also supported provided the IEEE P959 iSBX bus specification is followed.

NUMERIC DATA CO-PROCESSOR

The 80287 Numeric Data Co-Processor can be installed on the iSBC 286/100A board by the user. The 80287 Numeric Data Co-Processor is connected to dedicated processor signal lines which are pulled to their inactive state when the 80287 Numeric Data Co-Processor is not installed. This enables the user to detect via software that the 80287 socket is occupied. The 80287 Numeric Data Co-Processor runs asynchronously to the 80286 clock. The 80287 Numeric Data Co-Processor operates at 8 MHz and is driven by the 8284A clock generator.

Table 1. Interrupt Devices and Functions

Device	Function	Number of Interrupts
MULTIBUS® II Interface	Message-based Interrupt Request from the iPSB Bus via 84120 Message Interrupt Controller	1 Interrupt from up to 256 sources
8751 Interconnect Controller	BIST Control Functions	1
82530 Serial Controller	Transmit Buffer Empty, Receive Buffer Full and Channel Errors	1 Interrupt from 10 Sources
8254 Timers	Timers 0, 1, 2 Outputs; Function Determined by Timer Mode	3
8255A Parallel I/O	Parallel Port Control	2
iLBX II Bus Interface	Indicates iLBX™ II Bus Error Condition	3
iPSB Bus Interface	Indicates Transmission Error on iPSB Bus	1
iSBX Bus Connector	Function Determined by iSBX Bus MULTIMODULE Board	2
Edge Sense Out	Converts Edge Triggered Interrupt to a Level	1
Bus Error	Indicates Last iPSB Bus Operation Encountered an Error	1
Power-Fail	External/Power-Fail Interrupts	1

DMA CONTROL

Four DMA (Direct Memory Access) channels are supplied on the iSBC 286/100A board by the 82258. The 82258 is an advanced DMA controller designed especially for the 16-bit 80286 microprocessor. It has four DMA channels which can transfer data at rates up to 8 Megabytes per second (8 MHz clock) in an 80286 system. The large bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals.

MEMORY CAPABILITIES

The local memory of the iSBC 286/100A board consists of two groups of byte-wide sites. The first group of two sites are reserved for EPROM or ROM and are used for the BIST power-up diagnostic firmware. The second group of two sites support JEDEC standard 28-pin devices.

PARALLEL PERIPHERAL INTERFACE

The iSBC 286/100A board includes a parallel peripheral interface that consists of three 8-bit parallel ports. As shipped, these ports are configured for general purpose I/O. Programmed PAL (Programmable Array Logic) devices and the octal transceiver 74LS640-1 are provided to make it easy to reconfigure the parallel interface to be compatible with the SCSI (Small Computer System Interconnect) peripheral interface. Alternatively, the parallel interface may be reconfigured as a Centronics compatible line printer by adding one PAL and reconfiguring jumpers. Both interfaces may use the 82258 DMA controllers for data transfers.

The SCSI interface allows multiple mass storage peripherals such as Winchester disk drives, floppy disk drives, and tape drives to be connected directly to the iSBC 286/100A board. A sample SCSI application is shown in Figure 3. The SCSI interface is compatible with SCSI controllers such as the Adaptek 4500, DTC 1410, Iomga Alpha 10, Shugart 1601 and 1610, Vermont Research 8403, and Xebec 1410.

The Centronics interface requires very little software overhead since a user-supplied PAL device is used to provide necessary handshake timing. Interrupts are generated for printer fault conditions and a DMA request is issued for every character.

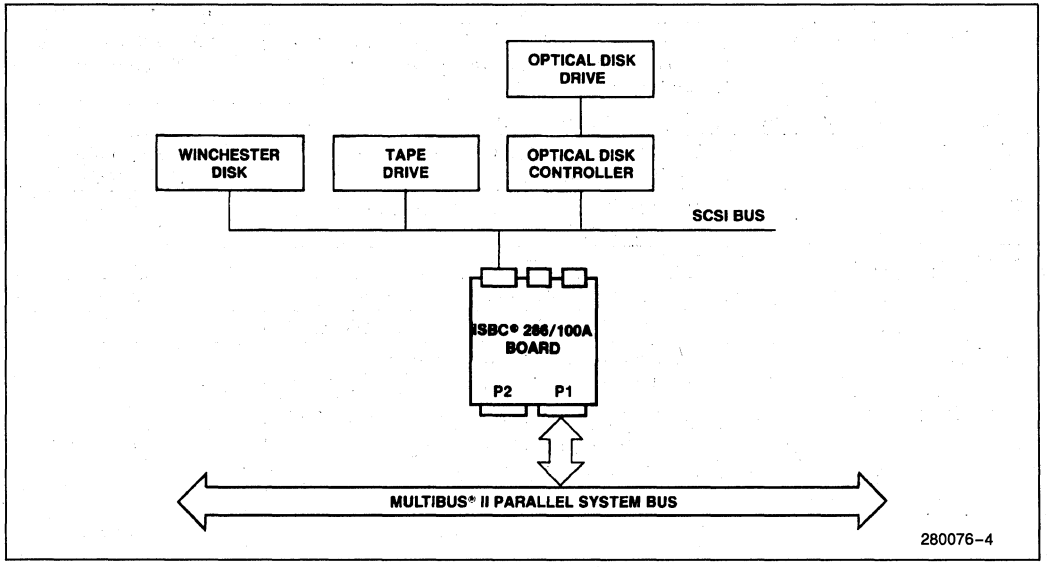

Figure 3. Sample SCSI Applications

SERIAL I/O

The 82530 Serial Communications Controller (SCC) is used to provide two channels of serial I/O. The SCC generates all baudrate clocks and provides loopback capability on both channels. Channel B is RS232C only and is configured as a DCE. Channel A is factory-default configured for DCE RS232C operation. Channel A may be reconfigured by the user for DTE or RS422 operation.

The 82258 ADMA can be programmed to support both channels A and B to perform movement of large bit streams or blocks of data.

PROGRAMMABLE TIMERS

The iSBC 286/100A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Three of these timers/counters are available to the system designer to generate accurate time intervals under software control. The outputs may be independently routed to the 8259A Programmable Interrupt Controller to count external events. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

SOFTWARE SUPPORT

The iRMX 86 Release 7 Operating System software provides the ability to execute all configurable layers of the iRMX 86 software in the MULTIBUS II environment. Applications in Real Address Mode are supported for the iSBC 286/100A board, including support for the SCSI peripheral interface and all iSBX bus boards. The iRMX 86 Release 7 Operating System also supports all 80286 component applications.

For on-target MULTIBUS II development, use the iSBX 218A or a SCSI controller and a floppy or Winchester drive, or port iRMX application software developed on the System 310, Series II/III, IV to MULTIBUS II hardware.

Language support for the iSBC 286/100A boards real address mode includes Intel's ASM 86, PL/M 86, PASCAL and FORTRAN as well as many third party 8086 languages. Language support for virtual address mode operation includes ASM 286, PL/M 286, PASCAL and C. Programs developed in these languages can be down-loaded from the Intel Series III or Series IV Development System to the iSBC 286/100A board via the iSDM 286 System Debug Monitor Release 2. The iSBX 218A can be used to load iRMX software developed on a System 310. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

Table 2. Programmable Time Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon request of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

The MULTIBUS II Interconnect Space Registers allow the software to configure boards eliminating much of the need for jumpers and wire wraps. The iSDM 286 Monitor can initialize these registers at configuration time using user-defined variables. The monitor can also automatically configure memory boards, defining the addresses for each board sequentially in relation to the board's physical placement in the card cage. This feature allows for swapping, adding, and deleting of memory boards on a dynamic basis.

SPECIFICATIONS

WORD SIZE

Instruction— 8-, 16-, 24-, 32-, or 40-bits

Data — 8- or 16-bits

SYSTEM CLOCK

CPU — 8.0 MHz

Numeric Co-Processor— 8.0 MHz

CYCLE TIME

Basic Instruction: 8.0 MHz-375 ns; 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles)

Memory Capacity (Maximum)

EPROM: 2732, 8K bytes; 2764, 16K bytes; 27128, 32K bytes; 27256, 64K bytes; 27512, 128K bytes

EEPROM: 2817A, 4K bytes

iRAM: 2186, 16K bytes

NOTE:
Two local sites must contain BIST or user-supplied boot-up EPROM.

I/O CAPABILITY

Parallel: SCSI, Centronics, or general purpose I/O

Serial: Two programmable channels using one 82530 Serial Communications Controller

Timers: Three programmable timers using one 8254 Programmable Interrupt Controller

Expansion: One 8/16-bit iSBX MULTIMODULE connector and one 8-bit iSBX MULTIMODULE connector

INTERRUPT CAPABILITY

Potential Interrupt Sources— 255 individual and 1 broadcast

Interrupt Levels — 16 vectored requests using two 8259As and the 80286 NMI line

Serial Communications Characteristics

Asynchronous Modes:

— 5–8-bit character; odd, even, or parity; 1, 1.5, or 2 stop bits

— Independent transmit and receive clocks, 1X, 16X, 32X, or 64X programmable sampling rate

— Error Detection: Framing, Overrun and Parity

— Break detection and generation

Bit Synchronous Modes:

— SDLC/HDLC flag generation and recognition

— Automatic zero bit insertion bit and detection

— Automatic CRC generation and detection (CRC 16 or CCITT)

— Abort generation and detection

— I-field residue handling

— SDLC loop mode operation

— CCITT X.25 compatible

Byte Synchronous Modes:

— Internal or external character synchronization (1 or 2 characters)

— Automatic CRC generation and checking (CRC 16 or CCITT)

— IBM Bisync compatible

Common Baud Rates

Baud Rate	Synchronous (x1 Clock)	Asynchronous (x16 Clock)
	Time Constant	Time Constant
64 K	36	—
48 K	49	—
19.2 K	126	6
9600	254	14
4800	510	30
2400	1022	62
1800	1363	83
1200	2046	126
300	8190	510
110	—	1394

Timers

Input Frequencies: 1.23 MHz ±0.1% or 4 MHz ±0.1% (Jumper Selectable)

Output Frequencies/Timing Intervals

	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	500 ns	53.1 ms	1.00 ms	57.9 min
Programmable One-Shot	500 ns	53.1 ms	1.00 ms	57.9 min
Rate Generator	18.8 Hz	2 MHz	0.000290 Hz	1 MHz
Square-Wave Rate Generator	18.8 Hz	2 MHz	0.000290 Hz	1 MHz
Software Triggered Strobe	500 ns	53.1 ms	1.00 ms	57.9 min
Hardware Triggered Strobe	500 ns	53.1 ms	1.00 ms	57.9 min
Event Counter	—	5.0 MHz	—	—

INTERFACES

iPSB Bus: All signals TTL compatible

iLBX II Bus: All signals TTL compatible

iSBX Bus: All signals TTL compatible

SERIAL I/O

Channel A: RS232C/RS422 compatible, configurable as a data set or data terminal

Channel B: RS232C compatible, configured as a data set

Timer: All signals TTl compatible

Interrupt Requests: All signals TTL compatible

CONNECTORS

Location	Function	Part #
P1	iPSB Bus	603-2-IEC-C096-F
P2	iLBX™ II Bus	603-2-IEC-C096-F

PHYSICAL DIMENSIONS

The iSBC 286/100A board meets all MULTIBUS II mechanical specifications as represented in the MULTIBUS II specification (part number 146077).

Double-High Eurocard Form Factor:

Depth:	220 mm (8.7 in.)
Height:	233 mm (9.2 in.)
Front Panel Width:	20 mm (0.784 in.)
Weight:	653 g (1 lb. 7 oz.)

ENVIRONMENTAL REQUIREMENTS

Temperature: (Inlet air) at 200 LFM airflow over boards

Non-operating—−40°C to +70°C

Operating—0 to +55°C

Humidity: Non-operating—95% RH @ 55°C

Operating—90% RH @ 55°C

ELECTRICAL CHARACTERISTICS

The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices, SCSI PALs, or expansion modules.

Voltage (volts)	Max/Typical Current (amps)	Max Power (watts)	BTU	Gram-Calorie
+5	10.31/8.25A	54.39W	3.13	774.2
+12	50/40 mA	630 mW	0.04	9.0
−12	46/37 mA	580 mW	0.03	8.3

REFERENCE MANUALS

ISBC 286/100A Single Board Manual Computer User's Guide (#149093-001)

Intel MULTIBUS II Bus Architecture Specification (#146077)

Manual may be ordered from any Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051

ORDERING INFORMATION

Part Number	Description
SBC 286/100A	MULTIBUS II 80286 based Single Board Computer